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BUR9-1999-0300US1
Amendment dated 07/27/2006

09/691,353

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Reply to office action mailed 02/23/2006

The following is a complete listing of all claims in the application, with an indication of the status of each:

Listing of claims:

- 1 1. (previously presented) A method of forming a field effect transistor (FET),
2 comprising:
3 providing a substrate;
4 forming a layer on the substrate, the layer having exposed vertical side
5 surfaces on opposite sides of the layer, the layer being able to support epitaxial
6 growth on said side surfaces;
7 forming an epitaxial channel on each of the exposed vertical side
8 surfaces of the layer, the channel having an exposed first vertical sidewall
9 opposite the vertical side surface of the layer;
10 removing a channel on a first vertical side surface of the layer and then
11 removing the layer, thereby exposing a second vertical sidewall of the channel
12 formed on the second vertical side of the layer;
13 forming a second channel in place of said removed channel; and
14 forming a gate adjacent to at least one of the sidewalls of the channel
15 and the second channel, there being a gate dielectric between each channel and
16 the gate.
- 1 2-23. (canceled)
- 1 24. (previously presented) A method of forming an FET, comprising:
2 forming on a substrate a first semiconductor layer having first and
3 second ends and a central region that is thinner than said first and second ends,
4 said central region having first and second side surfaces extending upward

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5 from said substrate, said semiconductor layer being able to support epitaxial
6 growth on said first and second side surfaces;
7 epitaxially growing a semiconductor channel region on at least one of
8 said first and second side surfaces of said central region of said first
9 semiconductor layer, a first side of said channel being exposed;
10 removing said central region of said first semiconductor layer, thereby
11 exposing a second side of said channel;
12 forming a dielectric layer on exposed surfaces of said semiconductor
13 channel region; and
14 forming a gate electrode on said dielectric layer.

1 25. (previously presented) The method of claim 24, wherein said
2 semiconductor channel region is formed of a combination of Group IV
3 elements.

1 26. (previously presented) The method of claim 24, wherein said
2 semiconductor channel region is formed of an alloy of silicon and a Group IV
3 element.

1 27. (previously presented) The method of claim 24, wherein said
2 semiconductor channel region is formed of a material selected from the group
3 consisting of silicon, silicon-germanium, and silicon-germanium-carbon.

1 28. (previously presented) The method of claim 27, wherein said step of
2 removing said first semiconductor layer does not appreciably remove said
3 semiconductor channel region.

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1 29. (previously presented) The method of claim 28, wherein an etch stop is
2 epitaxially grown between said first semiconductor layer and said
3 semiconductor channel region.

1 30 (previously presented) The method of claim 24, wherein said gate
2 electrode is formed of a material selected from the group consisting of
3 polysilicon, silicon-germanium, refractory metals, Ir, Al, Ru, Pt, and titanium
4 nitride.